CLAIM SET AS AMENDED

1. (currently amended) A data transmission and reception system comprising:

a data transmitter which multi-divides a transmission signal into a plurality of low-speed tributary signals, forms a frame for every tributary signal, thereafter multiplexes the tributary signals into a high-speed serial signal and transmits the high-speed serial signal through a transmission path; and

a data receiver which receives the serial signal through the transmission path, multi-divides the received serial signal into [[a]] the plurality of low-speed tributary signals, performs tributary synchronization with respect to every tributary signal, thereafter multiplexes the tributary signals into [[a]] the high-speed serial signal and reproduces the transmission signal,

wherein the data transmitter, when forming the frame for every tributary signal, inserts, into the frame a frame bit indicating a boundary of the frame and, after having formed the frame, performs only a bit synchronization with respect to every tributary signal, and

wherein the data receiver, for a respective tributary signal, stores a data indicated by the tributary signal and, in a timing based on a detection of the frame bit of the tributary signal and a reference frame pulse commonly issued between tributary signals,

outputs the stored 'data' to thereby perform the tributary synchronization.

2. (currently amended) The data transmission and reception system according to claim 1,

wherein the data transmitter comprises: ~~having,~~

a first serial-parallel conversion circuit which multi-divides the transmission signal into the plurality of tributary signals;

a coding circuit, for [[a]] the respective tributary signal, forms [[a]] the frame containing the frame bit and tributary ID information for identifying the tributary signal;

a delay circuit which performs the bit synchronization for a respective tributary signal of which the frame is formed by the coding circuit; and

a first parallel-serial conversion circuit which multiplexes the tributary signals, of which a respective one is processed for the bit synchronization by the delay circuit, into [[a]] the high-speed serial signal to be sent to the transmission path, and

wherein the data receiver comprises: ~~having,~~

a second serial-parallel conversion circuit which multi-divides [[a]] the high-speed serial signal received through the transmission path, into the plurality of tributary signals;

a tributary synchronization circuit which, for [[a]] the respective tributary signal, stores a data indicated by the

tributary signal and detects the tributary ID information and the frame bit of the tributary signal, to output the stored data in dependence on a detection of the frame bit and a reference frame pulse commonly issued between tributary signals;

a data replacement circuit which replaces the data indicated by tributary signals, of which a respective one is processed for [[a]] the tributary synchronization by the tributary synchronization circuit, in dependence on the tributary ID information;

a decoding circuit which, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, performs decoding corresponding to a coding by the coding circuit; and

a second parallel-serial conversion circuit which multiplexes the tributary signals, of which a respective one is decoded by the decoding circuit, into [[a]] the high-speed serial signal to reproduce the transmission signal.

3. (currently amended) The data transmission and reception system according to claim 2, wherein the tributary synchronization circuit comprises: ~~having,~~

a frame bit detector which detects the frame bit of [[a]] the respective tributary signal to output a frame pulse;

a reference frame pulse generator which generates the reference

frame pulse; and

a buffer which, for [[a]] the respective tributary signal, stores a data indicated by the tributary signal and, in a timing based on the frame pulse and the reference frame pulse, outputs the data with a match in phase of frame bits between tributary signals.

4. (currently amended) The data transmission and reception system according to claim 1,

wherein the data transmitter comprises: ~~having,~~

a first serial-parallel conversion circuit which multi-divides the transmission signal into [[a]] the plurality of tributary signals;

a coding circuit which, for [[a]] the respective tributary signal, forms the frame containing the frame bit and tributary ID information for identifying the tributary signal;

a delay circuit which performs the bit synchronization for [[a]] the respective tributary signal of which the frame is formed by the coding circuit; and

a first parallel-serial conversion circuit multiplexes the tributary signals, of which a respective one is processed for the bit synchronization by the delay circuit, into [[a]] the high-speed serial signal to be sent to the transmission path, and

wherein the data receiver comprises: ~~having,~~

a second serial-parallel conversion circuit which multi-divides

[[a]] the high-speed serial signal received through the transmission path, into [[a]] the plurality of tributary signals;

a data replacement circuit which performs replacement, between data indicated by the plurality of tributary signals, in dependence on a data replacement control signal;

a decoding circuit which, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, detects the frame bit of the tributary signal to output a frame pulse and for detecting the tributary ID information to output a tributary ID signal, to thereby perform a decoding of the tributary signal corresponding to a coding by the coding circuit;

a data replacement control circuit which decides whether or not the tributary ID information indicated by the tributary ID signal matches predetermined ID information, to be responsible for no match to output the data replacement control signal;

a tributary synchronization circuit which, for [[a]] the respective tributary signal, temporarily stores the data indicated by the tributary signal, and based on the frame pulse and a reference frame pulse commonly issued between tributary signals, outputs the stored data; and

a second parallel-serial conversion circuit which multiplexes the tributary signals, of which a respective one is processed for a tributary synchronization by the tributary synchronization circuit, into a high-speed serial 5 signal to reproduce the transmission

signal.

5. (currently amended) The data transmission and reception system according to claim 4, wherein, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, the decoding circuit comprises: ~~has,~~

a frame bit detector which detects the frame bit of the tributary signal to generate a frame pulse;

a tributary ID information detector which, in a timing based on the frame pulse, detects the tributary ID information of the tributary signal to generate a tributary ID signal; and

a decoder which performs, in a timing based on the frame pulse, for the tributary signal, decoding corresponding to a coding by the coding circuit, and outputs the frame pulse, the tributary ID signal, and the tributary signal for which the decoding is performed.

6. (currently amended) The data transmission and reception system according to claim 4,

wherein the tributary synchronization circuit comprises: ~~having,~~

a reference frame pulse generator which generates the reference frame pulse; and

a buffer which, for [[a]] the respective tributary signal,

stores the data indicated by the tributary signal in order in an address determined on bases of the frame pulse and a predetermined address for the frame bit to be written and, in a timing based on the reference frame pulse, outputs the data from the predetermined address.

7. (currently amended) The data transmission and reception system according to claim 2, wherein the data transmitter having, in place of the delay circuit, a bit synchronization circuit,

wherein said bit synchronization circuit, for [[a]] the respective tributary signal for which the frame is formed by the coding circuit, detects a phase slip of the tributary signal relative to a common clock signal between tributary signals and delays the tributary signal in accordance with the detected phase slip to thereby perform a bit synchronization.

8. (currently amended) The data transmission and reception system according to claim 4, wherein the data transmitter having, in place of the delay circuit, a bit synchronization circuit,

wherein said bit synchronization circuit, for [[a]] the respective tributary signal for which the frame is formed by the coding circuit, detects a phase slip of the tributary signal relative to a common clock signal between tributary signals and delays the tributary signal in accordance with the detected phase

slip to thereby perform a bit synchronization.

9. (currently amended) A data receiver which receives a high-speed serial signal through a transmission path, which serial signal is obtained by multi-dividing a transmission signal into a plurality of low-speed tributary signals, forming a frame for every tributary signal, thereafter multiplexing the tributary signals into a high-speed serial signal and transmitting the high-speed serial signal through the transmission path,

which data receiver multi-divides the received serial signal into [[a]] the plurality of low-speed tributary signals, performs tributary synchronization with respect to every tributary signal, thereafter multiplexes the tributary signals into [[a]] the high-speed serial signal and reproduces the transmission signal,

wherein the data receiver, for a respective tributary signal, stores a data indicated by the tributary signal and detects, from the tributary signal, a frame bit indicating a boundary of the frame, to output the stored data in a timing based on the detected frame bit and a reference frame pulse commonly issued between tributary signals, to thereby perform the tributary synchronization.

10. (currently amended) The data receiver according to claim 9, comprising:

a serial-parallel conversion circuit which multi-divides the high-speed serial signal received through the transmission path, into [[a]] the plurality of tributary signals;

a tributary synchronization circuit which, for [[a]] the respective tributary signal, stores the data indicated-by the tributary signal and detecting the frame bit of the tributary signal and tributary ID information for identifying the tributary signal, to output the stored data in dependence on a detection of the frame bit and a reference frame pulse commonly issued between tributary signals;

a data replacement circuit which performs replacement of data indicated by tributary signals, of which a respective one is processed for a tributary synchronization by the tributary synchronization circuit, in dependence on the tributary ID information;

a decoding circuit which, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, performs decoding; and

a parallel-serial conversion circuit which multiplexes the tributary signals, of which a respective one is decoded by the decoding circuit, into [[a]] the high-speed serial signal to reproduce the transmission signal.

11. (currently amended) The data receiver according to claim 10 ,

wherein the tributary synchronization circuit comprises: ~~having,~~

a frame bit detector detects the frame bit of [[a]] the respective tributary signal to output a frame pulse;

a reference frame pulse generator which generates the reference frame pulse; and

a buffer which, for [[a]] the respective tributary signal, stores the data indicated by the tributary signal and, in a timing based on the frame pulse and the reference frame pulse, outputs the data with a match in phase of frame bits between tributary signals.

12. (currently amended) The data receiver according to claim 9, comprising:

a serial-parallel conversion circuit which multi-divides the high-speed serial signal received through the transmission path, into a plurality of tributary signals;

a data replacement circuit which performs replacement, between data indicated by the plurality of tributary signals, in dependence on a data replacement control signal;

a decoding circuit which, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, detects the frame bit of the tributary signal to output a frame pulse and for detecting the tributary ID information to output a tributary ID signal, to thereby perform decoding of the tributary signal;

a data replacement control circuit which decides whether or not the tributary ID information indicated by the tributary ID signal matches predetermined ID information, to be responsible for no match to output the data replacement control signal;

a tributary synchronization circuit which, for [[a]] the respective tributary signal, temporarily stores a data indicated by the tributary signal, and based on the frame pulse and a reference frame pulse commonly issued between tributary signals, outputs the stored data; and

a parallel-serial conversion circuit which multiplexes the tributary signals, of which a respective one is processed for a tributary synchronization by the tributary synchronization circuit, into [[a]] the high-speed serial signal to reproduce the transmission signal.

13. (currently amended) The data receiver according to claim 12 , wherein ~~the decoding circuit has~~, for [[a]] the respective tributary signal for which the replacement is made by the data replacement circuit, the decoding circuit comprises:

a frame bit detector which detects the frame bit of the tributary signal to generate a frame pulse;

a tributary ID information detector which, in a timing based on the frame pulse, detects the tributary ID information of the tributary signal to generate [[a]] the tributary ID signal; and

a decoder which, in a timing based on the frame pulse, perform decoding, for the tributary signal, and outputs the frame pulse, the tributary ID signal, and the tributary signal for which the decoding is performed.

14. (currently amended) The data receiver according to claim 12 , wherein the tributary synchronization circuit comprises: ~~having,~~

a reference frame pulse generator which generates the reference frame pulse; and

a buffer which, for [[a]] the respective tributary signal, stores a data indicated by the tributary signal in order in an address determined on bases of the frame pulse and a predetermined address for the frame bit to be written and, in a timing based on the reference frame pulse, outputs the data from the predetermined address.

15. Cancelled